reverse blocking IGBT according to Embodiment 2. In FIG. **25**, the horizontal axis indicates the amount of charge stored in the interlayer insulating film **48** which selectively covers the front surface of the substrate in the edge termination structure region **100** and the vertical axis indicates a reverse breakdown voltage when a reverse voltage is applied. In the second examples (the effective total amount of impurity of the n-type high-concentration region **45** was 1.0×10^{11} cm^{-2}) and the comparative example, the reverse breakdown voltage was measured by a device simulation while changing the amount of charge in the interlayer insulating film **48**. The calculation result is illustrated in FIG. **25**. The length of the edge termination structure region **100** in the second example was substantially equal to the length of the edge termination structure region in the comparative example.

[0114] The result illustrated in FIG. **25** provided that, in the comparative example, a sufficiently high breakdown voltage was obtained when the amount of charge was about zero and the breakdown voltage was rapidly reduced when the amount of positive charge or negative charge stored in the interlayer insulating film of the edge termination structure region was greater than a predetermined value. In contrast, the result proved that, in the second examples, even when the positive charge or negative charge was stored in the interlayer insulating film **48** of the edge termination structure region **100**, it was possible to maintain the breakdown voltage that was substantially equal to that when the amount of charge was zero. Therefore, in the second examples, when the edge termination structure regions have substantially the same length, flexibility in the design is higher than that in the comparative example. The reverse blocking IGBT may have a charge resistance that is equal to or greater than a predetermined value, in order to ensure the long-term reliability of the edge termination structure region. Therefore, in the second examples, the structure of the edge termination structure region **100** is simplified and the length of the edge termination structure region **100** can be less than that in the comparative example.

[0115] As described above, according to Embodiment 2, even when the n-type high-concentration region is provided in the vicinity of the p collector region in the n drift region, instead of the n shell region, it is possible to obtain the same effect as that in Embodiment 1. In addition, according to Embodiment 2, since the n-type high-concentration region is provided in the vicinity of the p collector region in the n^- drift region, it is possible to adjust the reverse breakdown voltage so as to be close to the rated voltage. Therefore, it is possible to reduce the length of the edge termination structure region. According to Embodiment 2, the provision of the n-type high-concentration region makes it possible to improve the charge resistance while reducing the length of the edge termination structure region.

[0116] According to Embodiment 2, the provision of the n-type high-concentration region makes it possible to reduce the amount of forward leakage current. Furthermore, according to Embodiment 2, since the n-type high-concentration region is provided in the vicinity of the p collector region in the n^- drift region, it is possible to form a non-punch-through reverse blocking IGBT. Therefore, when the reverse blocking IGBT is turned off, the voltage waveform and the current waveform do not oscillate. In addition, according to Embodiment 2, it is not necessary to provide a trench in the rear surface of the substrate. Therefore, it is possible to simplify a manufacturing process and to manufacture a reverse blocking IGBT at a low cost.

[0117] The invention is not limited to the above-described embodiments, but various modifications and changes of the invention can be made without departing from the scope and spirit of the invention. For example, in each of the above-described embodiments, for example, the dimensions or surface concentration of each portion may be changed depending on required specifications. In addition, in Embodiment 2, a trench gate MOS structure may be provided instead of the planar gate MOS structure. Furthermore, in each embodiment, the n type and the p type may be reversed.

[0118] As described above, the semiconductor device according to the invention is useful for a power semiconductor device that is used as a switching device of a power conversion circuit, such as a matrix converter.

[0119] Thus, a semiconductor device has been described according to the present invention. Many modifications and variations may be made to the techniques and structures described and illustrated herein without departing from the spirit and scope of the invention. Accordingly, it should be understood that the devices and methods described herein are illustrative only and are not limiting upon the scope of the invention.

EXPLANATION OF LETTERS OR NUMERALS

[0120] **1**, **1***a* n^- drift region
[0121] **2**, **2***a* p base region
[0122] **2***b* p base region on rear surface side of substrate
[0123] **3**, **3***a* n^+ emitter region
[0124] **4**, **4***a* p^+ body region
[0125] **5** first trench
[0126] **5***a* second trench
[0127] **6**, **6***a* gate insulating film
[0128] **7**, **7***a* gate electrode
[0129] **8**, **8***a* insulating film, interlayer insulating film
[0130] **8***b* field insulating film
[0131] **9**, **9***a* emitter electrode
[0132] **10**, **10***a* p collector region
[0133] **11**, **11***a* collector electrode
[0134] **12** n LCS region
[0135] **13** n shell region (first shell region)
[0136] **13***a* n shell region (second shell region)
[0137] **14** field plate
[0138] **15** electrode on rear surface side
[0139] **20** p base junction
[0140] **21** collector junction
[0141] **21***a* ISOLATION region junction
[0142] **31***a* ISOLATION region
[0143] **100** edge termination structure region
[0144] **101** field limiting ring
[0145] **200** active region

What is claimed is:

1. A semiconductor device comprising:

a drift region that is a semiconductor substrate of a first conductivity type;

a base region of a second conductivity type that is selectively provided in a surface layer of a first main surface of the semiconductor substrate;

an emitter region of the first conductivity type that is selectively provided in the base region;